

FIG. 1

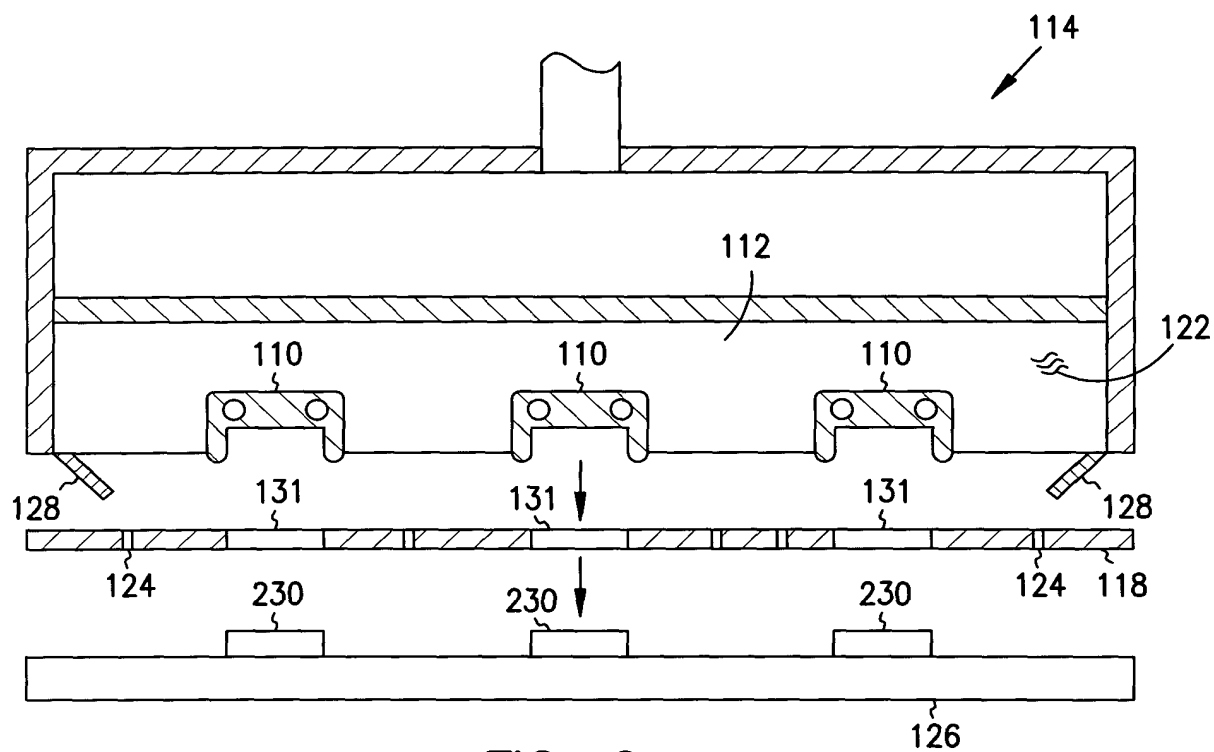
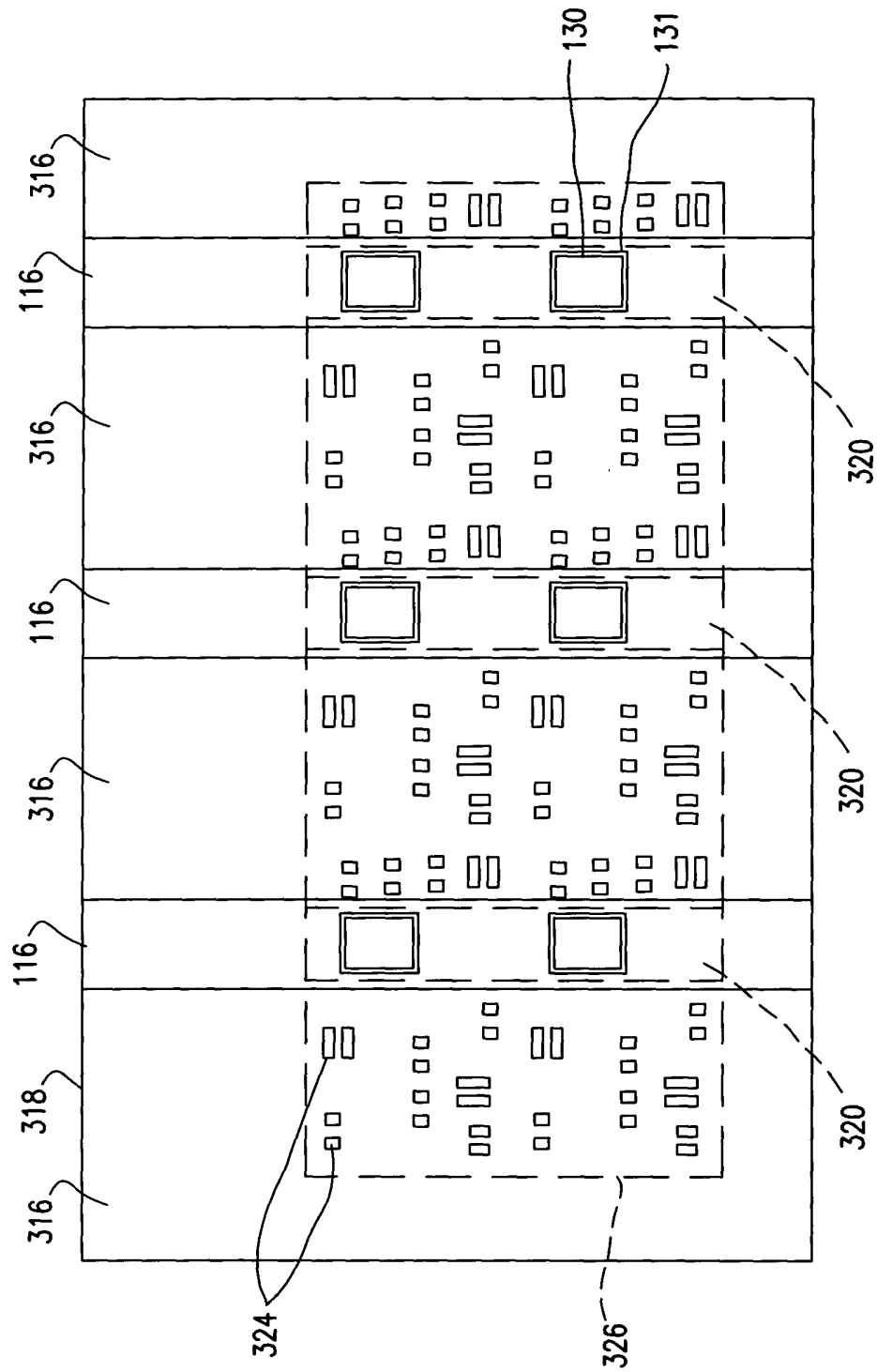


FIG. 2



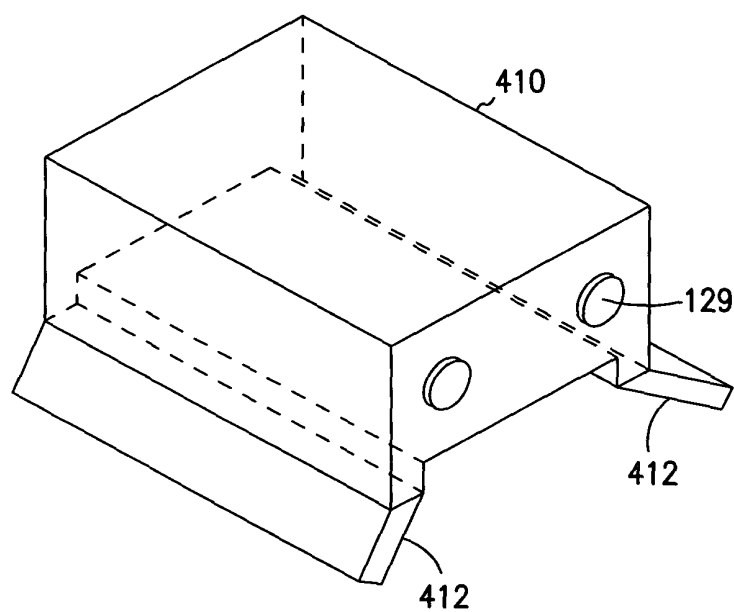


FIG. 4

CONTROLLED COLLAPSE CHIP CONNECTION PACKAGE PROCESS (C4 PACKAGE PROCESS)

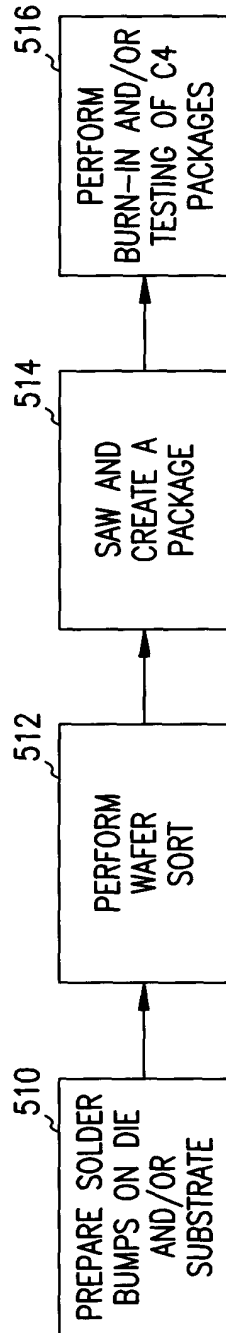


FIG. 5A (Prior Art)

FULL PRINTING AND PLACEMENT PROCESS

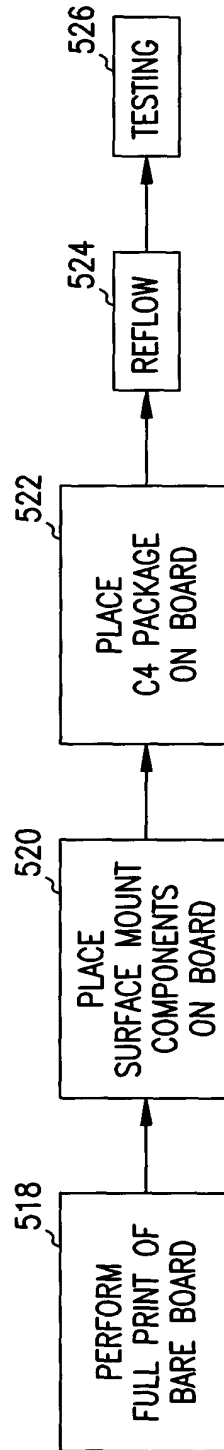


FIG. 5B (Prior Art)

PARTIAL PRINTING PROCESS

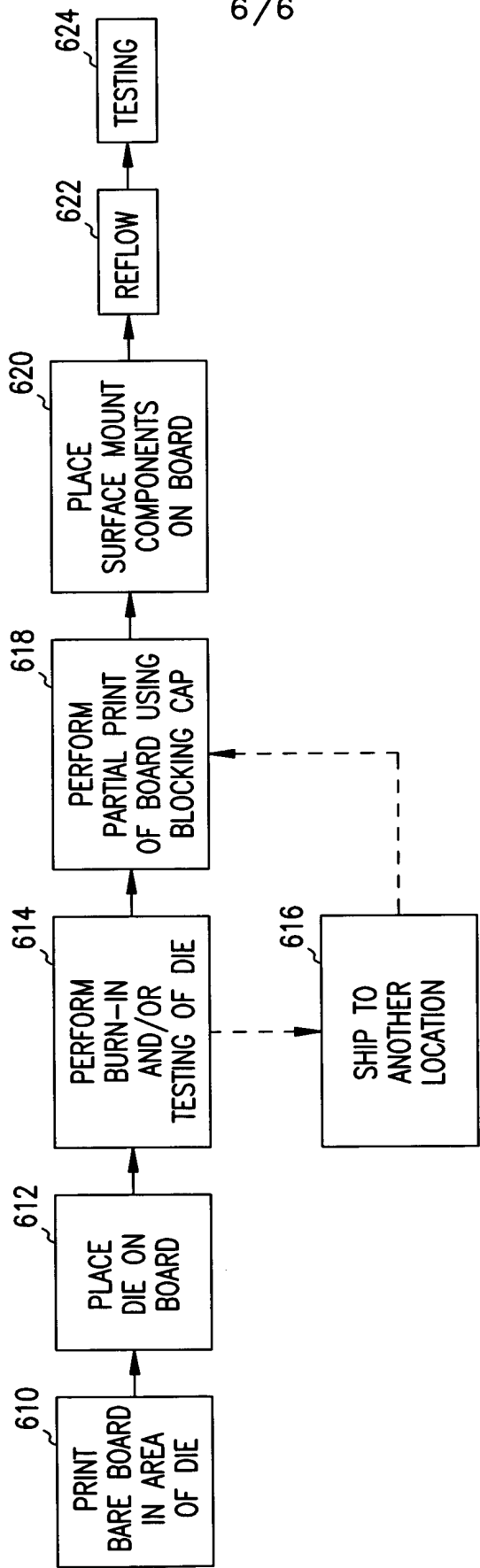


FIG. 6